ABSTRACT OF THE DISCLOSURE

A frequency multiplier circuit is provided that does not rely on filtering to remove unwanted harmonics and spurious content. In one implementation, a frequency doubler comprises a first rectifier doubler stage adapted to receive a first input signal having a first frequency and output a first rectified signal having multiple harmonics; a second rectifier doubler stage adapted to receive a second input signal having the first frequency and offset in phase from the first input signal and to output a second rectified signal, which has the multiple harmonics and is offset in phase from the first rectified signal; and a differential amplifier stage adapted to sum the first and second rectified signals to produce an output signal including a desired output harmonic having a frequency that is double the first frequency. The summing results in the substantial cancellation of unwanted output harmonics in the output signal.